Theory-Specific Proof Steps
Witnessing Correctness of SMT Executions

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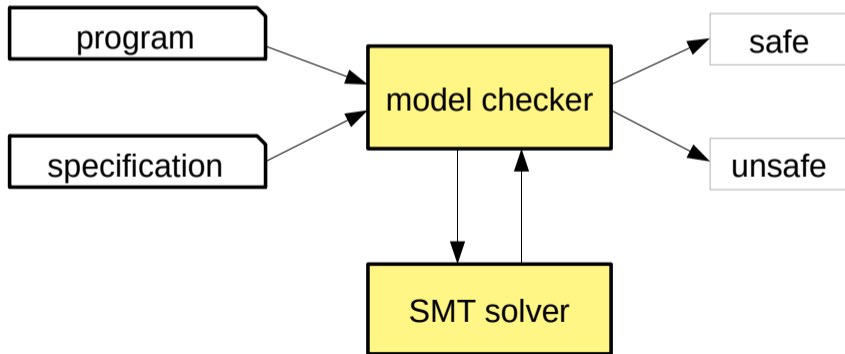[2] Charles University, Prague, Czech Republic
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State of the Art in Verification

- Software verification often relies on SMT solvers

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program

specification

model checker

safe

unsafe
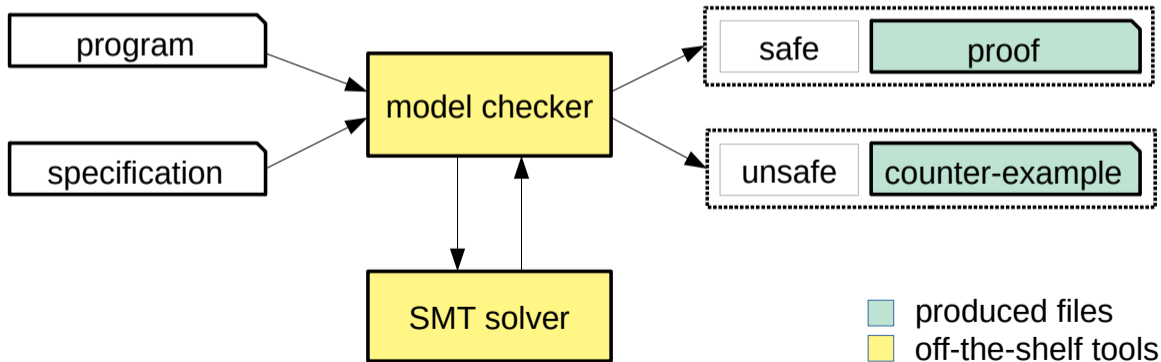
SMT solver

☐ off-the-shelf tools

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- At SMT-COMP'20, solvers disagreed on 149 instances with unknown status
- Guarantees are needed to trust solvers' results

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SMT solver

safe | proof

unsafe | counter-example

☐ produced files
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- The *de facto* standard for SAT proofs is the DRAT proof format
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Existing solver support

- Proofs validating SMT solvers' executions vary by implementation
  - Proof-producing solvers include CVC4, veriT, and Z3
- A commonality is the focus on integration with interactive theorem provers
  - SMT proofs can be consumed by Isabelle/HOL and Coq
- Current proof formats unsuitable to automation
  - Integration to automated tools such as model checkers is not available

Lightweight witnesses validating SMT solvers' executions

- Witnesses checkable by simple automated checkers
- Checkers simple enough to support manual inspection
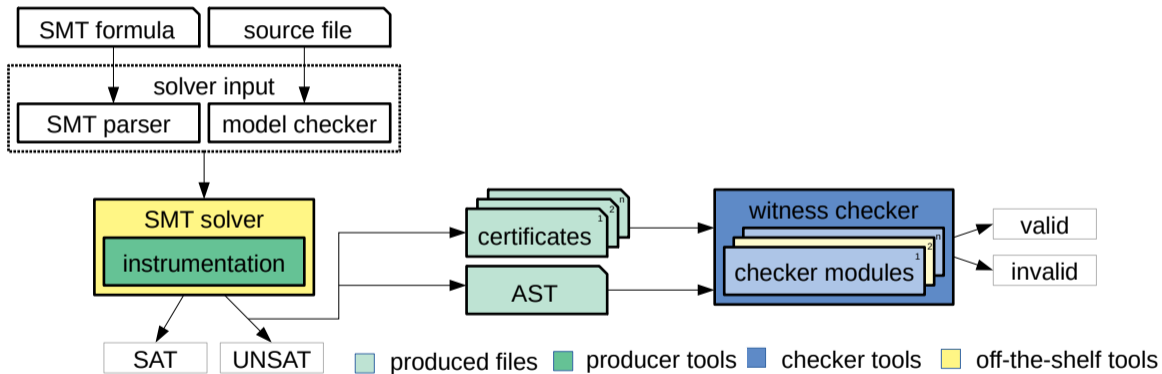- A user can write a checker in a few hours/days

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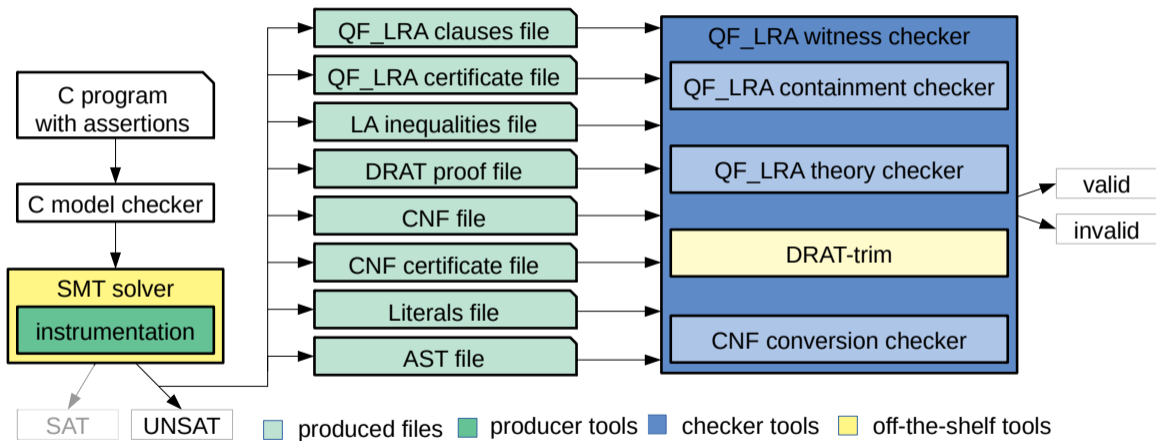- A user can write a checker in a few hours/days

Validation based on the foundations of SMT algorithms

- DRAT proofs for propositional logic
- Theory-specific witnesses for each supported SMT theory

```
1   float x = 1;
2   if ( condition ) {
3       x = x − 1;
4   } else {
5       x = x + 1;
6   }
7   assert ( x ≥ 0 );
```

$$x1 = 1 \wedge$$
$$(condition \rightarrow x4 = x2) \wedge x2 = x1 - 1 \wedge$$
$$(\neg condition \rightarrow x4 = x3) \wedge x3 = x1 + 1 \wedge$$
$$\neg(x4 \geq 0)$$

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$$(x4 \geq 0 \vee x4 < 2)$$

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$x4 < 0 \wedge x4 \geq 2$

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Witness
$x4 < 0 \land x4 \geq 2$

Validation			
$(1x)$	$-x4$	$>$	0
$(1x)$	$x4$	$\geq$	2
	0	$>$	2

Checking Architecture

- **produced files** (green)
- **checker tools** (blue)
- **off-the-shelf tools** (yellow)

Files and tools shown in the diagram:

- CNF conversion / CNF conversion checker → DAG file, CNF certificate file
- CNF file
- SAT solving / DRAT-trim → DRAT proof file
- literals file
- LA inequalities file
- QF_LRA certificate file
- QF_LRA clauses file
- QF_LRA solving / QF_LRA theory checker / QF_LRA containment checker
- QF_UF solving / QF_UF theory checker / QF_UF containment checker → QF_UF terms file, QF_UF certificate file, QF_UF clauses file
- QF_LIA solving / QF_LIA real theory checker / QF_LIA real containment checker / QF_LIA integer theory checker / QF_LIA integer containment checker
- QF_LIA certificate file
- QF_LIA clauses file

Our tools

- Witness production implemented in the OpenSMT solver
- New Theory-Specific Witness Checker (TSWC)

Evaluation

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Evaluation setup

- All non-incremental SMT-LIB instances for the QF_LRA, QF_LIA, and QF_UF theories
- Witness-production comparison against CVC4, veriT, Z3
- Witness-checking comparison against CVC4's LFSC checker

Witness Production Results

		UNSAT retention (%)	Avg. runtime (s)	Avg. witness size (MB)
	OPENSMT	**99.5%**	**3.91/4.31**	3.9
QF_LRA	CVC4	97.7%	5.73/6.61	13.6
(1648 instances)	VERIT	96.7%	4.12/5.22	69.4
	Z3	97.8%	5.17/5.30	**3.5**
	OPENSMT	75%	10.07/9.99	**13.0**
QF_LIA	CVC4	66.3%	6.30/**1.30**	18.8
(6947 instances)	VERIT	95.1%	**1.82**/4.05	165.9
	Z3	**104.5%**	5.17/6.62	24.8
	OPENSMT	**99.6%**	0.95/1.14	**6.7**
QF_UF	CVC4	97.6%	0.39/1.83	6.8
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- Witnesses for parallel SMT solving
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- Details about this work can be found on our DAC'21 paper
- Check our group's website for future updates

`verify.inf.usi.ch/research/cevt`